REMARKS

Claims 1-23 and 35-40 are currently pending in this application.

Applicants graciously acknowledge the allowance of claims 19-23. Since claims 39 and 40 depend from allowed claim 19 and are not rejected or objected to by the Examiner, Applicants assume that claims 39 and 40 are also allowed.

Claims 1-3, 5-8, 10-16, and 18 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Corisis, US Patent No. 6,163,956 ("Corisis"). This rejection is respectfully traversed.

The present invention relates to methods of making semiconductor packages. Independent claims 1 and 11 recite a "method of making semiconductor device packages." The method according to independent claim 1 comprises, *inter alia*, "testing semiconductor devices in said wafer" and "subsequently, dicing said layered assembly." The method according to independent claim 11 comprises, *inter alia*, "providing conductive structures in contact with a top surface of a dielectric substrate," "subsequently, forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to said dielectric substrate," and "subsequently, dicing said layered assembly."

Corisis fails to disclose all limitations of any of independent claims 1 and 11. Corisis relates to a chip-on-board semiconductor device assembly with a heat spreading/dissipating member. Corisis at col. 1, lines 12-15. With reference to independent claim 1, Corisis fails to disclose "testing semiconductor devices in said wafer" and "subsequently, dicing said layered assembly." Instead, Corisis teaches producing a plurality of semiconductor dice with integrated assembly as a wafer, then separating the individual die from the wafer. After separation, each die is individually

bonded to a paddle of a paddle frame. The dice are then tested while connected to the paddles. Corisis at col. 4, lines 33-67. Therefore, Corisis does not disclose all limitations of independent claim 1.

Likewise, Corisis does not disclose all limitations of independent claim 11. Specifically, Corisis fails to disclose "providing conductive structures in contact with a top surface of a dielectric substrate," "subsequently, forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to said dielectric substrate," and "subsequently, dicing said layered assembly." Corisis discloses conductive traces 46 of a substrate 42 comprising a circuit board. According to Corisis, semiconductor device assemblies 40 are bonded to the substrate 42 after the semiconductor device assemblies are singulated from the paddle frame 12, which Corisis discloses occurs after the individual die are separated from the wafer. Corisis at col. 4 line 33 - col. 5, line 7. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 9 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis in view of Takahashi, US Patent No. 6,153,448 ("Takahashi"). This rejection is respectfully traversed.

Applicant respectfully submits that Corisis is not a valid reference under 35 U.S.C. §103(a) pursuant to 35 U.S.C. §103(c). The subject matter of Corisis qualifies as a prior art reference only under 35 U.S.C. §102(e). At the time the present invention was made and filed, the subject matter of Corisis and the present invention were owned by or subject to an obligation of assignment to Micron Technology, Inc. A copy of the assignment of the subject matter of Corisis to Micron Technology, Inc. is attached hereto. Therefore, pursuant to 35 U.S.C. §103(c), the subject matter of Corisis cannot preclude the patentability of the present invention. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis in view of Smith, US Patent No. 6,064,217 ("Smith"). This rejection is respectfully traversed.

As noted above, pursuant to 35 U.S.C. § 103(c) Corisis cannot support a rejection of the present application under 35 U.S.C. § 103(a). For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 35 and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam, US Patent No. 6,3344,401 ("Lam") in view of Kobayashi, US Patent No. 4,781,969 ("Kobayashi"). Applicants respectfully traverse this rejection and request reconsideration.

The claimed method includes the step of "adhering said wafer to a flexible substrate." Neither Lam nor Kobayashi teach or suggest such a step. As noted by the Office Action, Lam is silent about adhering a wafer to a flexible substrate. Office Action at 6. The Examiner asserts that Kobayashi discloses a printed circuit board "with (35).....adhering said wafer to a flexible substrate." Office Action at 6. Kobayashi, however, discloses affixing a composite metal layer, not a wafer, to a flexible substrate. Kobayashi at col. 1, lines 38-43. Claim 37 depends from independent claim 35 and is believed to be allowable for at least the same reasons.

Claims 36 and 38 are rejected under 35 U.S.C. § 103(a) as being obvious over Lam in view of Kobayashi and in further view of Lam, US Patent No. 5,137,836 ("Lam '836"). Applicants respectfully traverse this rejection and request reconsideration.

As noted above, Lam and Kobayashi, even when considered in combination, fail to teach or suggest all limitations of independent claim 35. Lam '836 is cited in the

Office Action for other reasons. Claims 36 and 38 depend from independent claim 35 and are believed to be allowable for at least the same reasons.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: July 27, 2004

Respectfully submitted,

By_____

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Attachment

PATENT
Attorney Docket No. 3384US (97-564)

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, each undersigned ASSIGNOR does hereby:

SELL, ASSIGN AND TRANSFER to MICRON TECHNOLOGY, INC. ("ASSIGNEE"), a corporation of the State of Delaware having a place of business at 8000 South Federal Way, Boise, Idaho 83707-0006, the entire right, title and interest for the United States and all foreign countries in and to any and all improvements which are disclosed in the Application for United States Letters Patent which has been executed by each undersigned ASSIGNOR concurrently herewith and is entitled **CHIP SCALE PACKAGE WITH HEAT SPREADER AND METHOD OF MANUFACTURE**, such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original, reissued and reexamined patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the ASSIGNEE;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT, when requested and at the expense of the ASSIGNEE, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the ASSIGNEE all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the ASSIGNEE shall consider desirable for vesting title to such improvements in the ASSIGNEE, and for securing, maintaining and enforcing proper patent protection for such improvements;

Attorney Docket No. 3384US (97-564)

TO BE BINDING on the heirs, assigns, representatives and successors of each undersigned ASSIGNOR and extend to the successors, assigns and nominees of the ASSIGNEE.

ASSIGNORS:

David J. Corisis Date 2/19/98

STATE OF IDAHO)
: ss.
County of Ada)

BEFORE ME, the undersigned authority, on this 19th day of February, 1998, personally appeared David J. Corisis, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he executed the same of his of own free will for the purposes and consideration therein expressed.

KERRI LEICHTON NOTARY PUBLIC STATE OF IDAHO

Notary or Consular Officer